

2 a plurality of p-channel transistors formed in active surface areas of n-type regions, wherein
3 the p-channel transistors do not have LDD source/drain regions;

4 a plurality of n-channel transistors formed in isolated active surface areas of p-type regions;
5 gate electrodes for the p-channel and n-channel transistors, the gate electrodes overlying and
6 being insulated from the respective active surface areas, wherein the gate electrodes for the p-channel
7 transistors have a width less than a minimum channel length required for the p-channel transistors;

8 p-type source and drain regions for the p-channel transistors, each p-type source and drain
9 region consisting of a low resistivity region;

10 n-type source and drain regions for the n-channel transistors, each n-type source and drain
11 region having a low resistivity region and an LDD region;

12 each gate electrode having a pair of sidewall spacers each having an inner and an outer
13 portion, wherein the inner portions of the sidewall spacers for each p-channel transistor gate
14 electrode has a width which, taken on each side of the respective gate electrode for the respective
15 p-channel transistor and combined with the width of the respective gate electrode for the respective
16 p-channel transistor, exceeds a minimum channel length for the respective p-channel transistor;

17 each p-channel low resistivity region located under the outer portion and at least a part of the
18 inner portion of its respective sidewall spacer;

19 each n-channel low resistivity region located under at least a part of the outer portion and a
20 part of the inner portion of its respective sidewall spacer; and

21 each n-channel LDD region extending from its respective low resistivity region to underlie
22 the inner portion of its respective sidewall spacer.

1 2. (Unchanged/Original) The integrated circuit of claim 1, wherein the inner portion of the sidewall
2 spacer comprises an oxide.

1 3. (Unchanged/Original) The integrated circuit of claim 1, wherein the inner portion of the sidewall
2 spacer comprises an oxide.

1 4. (Unchanged/Original) The integrated circuit of claim 1, wherein the p-channel source and drain
2 comprise silicon implanted with BF_2 .

1 5. (Previously Amended) The integrated circuit of claim 1, wherein:

2 the distance between low resistivity regions of the source and drain regions of the p-channel
3 transistor is between the p-channel minimum length and the p-channel maximum length, wherein:

4 the p-channel minimum length is a distance below which the transistor will not
5 operate reliably due to short channel effects; and

6 the p-channel maximum length is a distance above which the transistor will not turn
7 on efficiently.

1 6. (Previously Amended) The integrated circuit of claim 1, wherein:

2 the distance between the low resistivity regions of the n-channel transistor is between the n-
3 channel minimum LDD length and the n-channel maximum LDD length, wherein:

4 the n-channel minimum LDD length is a distance below which the transistor will not
5 operate reliably due to short channel effects; and

6 the n-channel maximum LDD length is a distance above which the transistor will not
7 turn on efficiently.

1 7. (Unchanged/Original) The integrated circuit of claim 1, wherein the sidewall spacers have a total
2 width of approximately 500 to 2500 Å.

Claims 8-26 previously canceled.

1 27. (Currently Amended) A CMOS integrated circuit structure, comprising:

2 an n-channel transistor including lightly doped source and drain regions within a p-type
3 region of a substrate; and

4 a p-channel transistor without lightly doped source and drain regions within an n-type region
C1 5 of the substrate, the p-channel transistor including:

6 a gate electrode having a width less than a channel length of a channel for the p-
7 channel transistor; and

8 first and second sidewall spacer[s] regions adjacent opposing sides of the gate
9 electrode and overlying a portion of the channel for the p-channel transistor and portions of
10 source and drain regions for the p-channel transistor.

1 28. (Currently Amended) A CMOS integrated circuit structure, comprising:

2 an n-channel transistor including lightly doped source and drain regions within a p-type
3 region of a substrate; and

4 a p-channel transistor without lightly doped source and drain regions within an n-type region
5 of the substrate, the p-channel transistor including:

6 a gate electrode having a width less than a channel length of a channel for the p-
7 channel transistor; and

8 first sidewall spacer regions adjacent opposing sides of the gate electrode and
9 overlying at least a portion of the channel for the p-channel transistor and portions of source
10 and drain regions for the p-channel transistor,

11 wherein the width of the gate electrode is less than a minimum channel length required for
12 the p-channel transistor.

1 29. (Currently Amended) The CMOS integrated circuit structure of claim 28, wherein the first
2 sidewall spacer regions have a width which, taken on opposing sides of the gate electrode and
3 combined with the width of the gate electrode, exceeds the minimum channel length required for the
4 p-channel transistor.

sub 07
1 30. (Currently Amended) The CMOS integrated circuit structure of claim 29, wherein the width of
2 the first sidewall spacer regions, taken on opposing sides of the gate electrode and combined with
3 the width of the gate electrode, exceeds the minimum channel length required for the p-channel
4 transistor plus a diffusion distance for implanted dopants forming source and drain regions for the
5 p-channel transistor.

C2
cont.
1 31. (Currently Amended) The CMOS integrated circuit structure of claim 30, further comprising:
2 second sidewall spacer regions adjacent the first sidewall spacer regions and overlying source
3 and drain regions for the p-channel transistor.

1 32. (Unchanged/Previously Added) The CMOS integrated circuit structure of claim 30, wherein the
2 n-channel transistor further comprises:
3 a gate electrode having a width approximately equal to a minimum channel length required
4 for the n-channel transistor; and
5 sidewall spacers adjacent to opposing sides of the n-channel transistor gate electrode and
6 overlying the lightly doped source and drain regions.

1 33. (Previously Amended) An intermediate structure for use in forming a CMOS integrated circuit,
2 comprising:

3 a p-type region for an n-channel transistor including lightly doped source and drain regions;
4 an n-type region for a p-channel transistor without lightly doped source and drain regions;
5 a gate electrode overlying a portion of the n-type region, the gate electrode having a width
6 less than a minimum channel length required for the p-channel transistor; and

7 at least one conformal insulating layer over a top and sides of the gate electrode, the
8 insulating layer having a thickness which, taken on opposing sides of the gate electrode and
9 combined with the width of the gate electrode, exceeds a minimum channel length required for the
10 p-channel transistor.

1 34. (Unchanged/Previously Added) The intermediate structure of claim 33, wherein the insulating
2 layer forms a mask for implanting source and drain regions for the p-channel transistor.

1 35. (Unchanged/Previously Added) The intermediate structure of claim 34, wherein the insulating
2 layer has a thickness which, taken on opposing sides of the gate electrode and combined with the
3 width of the gate electrode, exceeds the minimum channel length required for the p-channel
4 transistor plus a diffusion distance for implanted dopants forming the source and drain regions for
5 the p-channel transistor.

1 36. (Unchanged/Previously Added) The intermediate structure of claim 35, further comprising:
2 source and drain regions for the p-channel transistor within the n-type region, wherein edges
3 of the source and drain regions are spaced apart from the sides of the gate electrode.

1 37. (Unchanged/Previously Added) The intermediate structure of claim 36, wherein the source and
2 drain regions are low resistivity regions.

1 38. (Unchanged/Previously Added) The intermediate structure of claim 33, further comprising:
2 second insulating layer overlying the first insulating layer to form sidewall spacers adjacent
3 the gate electrode upon etching of the insulating layer and the second insulating layer.

1 39. (Unchanged/Previously Added) The intermediate structure of claim 33, further comprising:
2 a n-channel transistor gate electrode overlying a portion of the p-type region;
3 lightly doped source and drain regions within the p-type region aligned with the n-channel
4 transistor gate electrode.